

**REMARKS**

This is in full and timely response the non-final Office Action mailed on February 25, 2004. Reexamination in light of the following remarks is respectfully requested.

Claims 13-25 are currently pending in this application, with claim 13 being independent. No new matter has been added.

**Drawing objections**

In response to the objection to the drawings, drawings are being provided herewith that include figures 1 and 2 having a legend such as -- Related Art --. Withdrawal of this objection is respectfully requested.

**Specification objection**

While not conceding the propriety of this objection to the title and to advance the prosecution of the above-identified application, the title has been amended. Withdrawal of this objection is respectfully requested.

**Rejections under 35 U.S.C. §102 and §103**

While not conceding the propriety of these rejections, and in order to further the prosecution of the application, claims 1-12 have been canceled without prejudice or disclaimer of their underlying subject matter, rendering the rejection moot as to these claims. Withdrawal of these rejections is respectfully requested.

**Newly added claims**

Newly added claim 13 and the claims dependent thereon include the features of:

a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits,

one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory,

one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide,

another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory,

another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide; and

a central processing unit receiving said plurality of coincidence signals, wherein said central processing unit:

executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses,

executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses, and

executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses.

U.S. Patent No. 5,454,100 to Sagane arguably teaches an electronic apparatus. If the ROM 3 of Sagane includes a plurality of bugs to be corrected, Sagane arguably teaches that step S10 of figure 2 may be followed for each bug by a step of updating the interrupt generating address register 9 and the interrupt vector register 7b to reflect the next correction address and the start address of the next correction content, respectively (figure 1, column 5, lines 49-54).

Yet, Sagane as related to figure 1 fails to disclose, teach or suggest a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits.

Sagane arguably teaches that step S31 of figure 4 may be followed for each bug by a step of updating the correction address register 21 and the correction data register 22 to reflect the next correction address and the next correction data, respectively (column 6, lines 63-67).

Nevertheless, this feature of Sagane fails to disclose, teach or suggest a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits.

While figure 3 of Sagane arguably teaches a single central processing unit 2, a single comparator 8, a single correction address register 21 and a single correction data register 22, Sagane arguably teaches that a pluralities of comparators 8, correction address registers 21 and correction data registers 22 may be provided to address the multiple bugs (figure 3, column 7, lines 1-3).

However, Sagane fails to disclose, teach or suggest the central processing unit 2 as receiving a plurality of coincidence signals (figures 1 and 3).

Regarding the related art disclosed within the specification for the above-identified application, figure 2 arguably depicts a debugging circuit 20.

But figure 2 of the related art fails to disclose, teach or suggest the debugging circuit 20 as having a plurality of bug address setting registers and a plurality of coincidence detecting circuits, and figure 1 of the related art fails to disclose, teach or suggest the central processing unit 10 as receiving a plurality of coincidence signals.

Allowance of the claims is respectfully requested.

### **Conclusion**

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. (original) Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

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Respectfully submitted,

By 

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